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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/618,508 | 07/11/2003 | Kazutaka Manabe | N09692401WD1 | 6561 |
| 7590 | 02/07/2005 | | EXAMINER | |
| Darryl G. Walker WALKER & SAKO, LLP Suite 235 300 South First Street San Jose, CA 95113 | | | MENZ, DOUGLAS M | |
| | | ART UNIT | PAPER NUMBER | |
| | | | 2829 | |
| DATE MAILED: 02/07/2005 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|------------------------------|------------------------|---------------------|--|
| | 10/618,508 | MANABE, KAZUTAKA | |
| | Examiner | Art Unit | |
| | Douglas M. Menz | 2824 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 January 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-8 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 11 July 2003 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: *Search History*

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I, claims 1-8, in the reply filed on 1/4/05 is acknowledged.

Claim Rejections - 35 USC § 112

Claims 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "second gate electrode" in line two. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "second gate electrode" in line two. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaya et al. (US 5821581).

Regarding claim 1, Kaya discloses a semiconductor device, comprising:

an insulated gate field effect transistor (8, Figs. 1, 7d and 7e) including

a first source/drain area (14) of a second conductivity type formed in a semiconductor area (10) of a first conductivity type;

a second source/drain area (12) of the second conductivity type formed in the semiconductor area (10); and

a gate electrode (22) formed on a gate insulating film on a channel area (16) disposed between the first source/drain area (14) and the second source/drain area (12), the gate insulating film includes a first gate insulating film (26) formed on a first channel area portion (16b) and a second gate insulating film (20) formed on a second channel area portion (16a) wherein

a second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area (Col. 7, lines: 43-51) and a thickness of the first gate insulating film (26) is different from a thickness of the second gate insulating film (20, Figs. 1, 7d, 7e and Col. 3).

Regarding claim 2, Kaya further discloses wherein a first type impurity concentration distribution in the first channel area portion (16b) is different from the first

type impurity concentration distribution in the second channel area portion (16a, Figs. 1, 7d, 7e and Col. 3, lines: 55-65).

Regarding claim 3, Kaya further discloses wherein the first gate electrode (22) and the second gate electrode (18) are formed in a sidewall configuration (Figs. 1, 7d and 7e).

Regarding claim 5, Kaya further discloses wherein an insulating film (24) is formed between the first gate electrode (22) and the second gate electrode (18, Figs. 1, 7d and 7e).

Regarding claim 6, Kaya further discloses wherein the first channel area portion (16b) is adjacent to the first source/drain area (14) and the second channel area portion (16a) is adjacent to the second source/drain area (12) (Figs. 1, 7d and 7e),

wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area (Col. 7, lines: 43-50)

and the first gate insulating film (26) is thicker than the second gate insulating film (20) (Figs. 1, 7d, 7e and Col. 3).

Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US 5600168).

Regarding claim 1, Lee discloses a semiconductor device, comprising:

an insulated gate field effect transistor (Fig. 3) including

a first source/drain area (26) of a second conductivity type formed in a semiconductor area (1) of a first conductivity type;

a second source/drain area (24) of the second conductivity type formed in the semiconductor area (1); and

a gate electrode (17) formed on a gate insulating film on a channel area disposed between the first source/drain area (26) and the second source/drain area (24), the gate insulating film includes a first gate insulating film (16) formed on a first channel area portion and a second gate insulating film (18) formed on a second channel area portion (Fig. 3 and Col. 4) wherein

a second type impurity concentration distribution in the first source/drain area (26) is different from the second type impurity concentration distribution in the second source/drain area (24) (Fig. 3 and Col. 6, lines: 1-20) and a thickness of the first gate insulating film (16) is different from a thickness of the second gate insulating film (18, Fig. 3 and Col. 4, lines: 35-40).

Regarding claim 4, Lee further discloses wherein the first gate electrode (17) and second gate electrode (21) are electrically connected through a third gate electrode (22) (Fig. 3 and Col. 4, lines: 10-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaya et al. (US 5821581).

Regarding claim 7, Kaya discloses the structure of claim 1 as mentioned above, and further discloses wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area (Col. 7, lines: 43-50) and that the source/drain region is electrically connected to a bit line (Fig. 2). Kaya does not explicitly disclose a capacitor electrically connected to the first source/drain area, however, this is a common configuration which was well known in the art at the time of the invention and would therefore have been obvious to one of ordinary skill in the art at that time.

Regarding claim 8, Kaya further discloses wherein the second source/drain area provides a common source/drain area for a pair of memory cells (Col. 4, lines: 60-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas M. Menz whose telephone number is 571-272-1877. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM



BRADLEY BAUMEISTER
PRIMARY EXAMINER